

	Search Text
1	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031"
2	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" (chang\$4 modif\$7 custom\$7 var\$8 subdivi\$7 reconfig\$6) with ( memor\$4 dram ram sram rom erom eerom eeprom flash)
3	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" and (chang\$4 modif\$7 custom\$7 var\$8 subdivi\$7 reconfig\$6)
4	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" and (chang\$4 modif\$7 custom\$7 var\$6 subdivi\$7 reconfig\$6) with ( memor\$4 dram ram sram rom erom eerom eeprom flash) and layout\$4 and (fixed dedicat\$4) with (core macro logic controller processor microprocessor micro adj processor)
5	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" and (chang\$4 modif\$7 custom\$7 var\$6 subdivi\$7 reconfig\$6) with ( memor\$4 dram ram sram rom erom eerom eeprom flash) and layout\$4 and (fixed dedicat\$4) with (core macro logic controller processor microprocessor micro adj processor) and timing near2 (anal\$5 verif\$4 simulat\$4)
6	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" and (chang\$4 modif\$7 custom\$7 var\$6 subdivi\$7 reconfig\$6) with ( memor\$4 dram ram sram rom erom eerom eeprom flash) and layout\$4 and (fixed dedicat\$4) with (core macro logic controller processor microprocessor micro adj processor) and timing near2 (anal\$5 verif\$4 simulat\$4) and layout\$4 with (chang\$4 var\$4 modif\$5)
7	( memor\$4 dram ram sram rom erom eerom eeprom flash) with (var\$5 grow\$4 add\$4 expan\$6 exten\$5) and @ad<="20021031" and (chang\$4 modif\$7 custom\$7 var\$6 subdivi\$7 reconfig\$6) with ( memor\$4 dram ram sram rom erom eerom eeprom flash) and layout\$4 and (fixed dedicat\$4) with (core macro logic controller processor microprocessor micro adj processor) and timing near2 (anal\$5 verif\$4 simulat\$4) and layout\$4 with (chang\$4 var\$4 modif\$5) and "716"/\$.ccls.